Design and Robustness Evaluation of a 7nm FinFET DICE SRAM

Maria Eduarda de Melo Hang and Cristina Meinhardt
Departamento de Informática e Estatistica, PPGC, Universidade Federal de Santa Catarina
Email: maria.eduarda.melo.hang@gmail.com, cristina.meinhardt@ufsc.br

***Abstract*—This work shows the design and evaluation of Dual Interlocked Cell (DICE) in FinFET 7nm technology in terms of read and write times, energy consumption, tolerance to SEU and noise margins, considering the voltage scale technique. Even with an aggressive voltage scaling, the DICE circuit remains more robustness compared with 6T operating at 0.4V, shows a reduction of 58% on the LETth and 33% on the Read Static Noise Margin compared with the DICE nominal operation.**

***Index Terms*—SRAM, nanotechnology, DICE, Noise Margin, SEU, Single-Event-Upset, FinFET**

I. Introduction

The memory system still being a significant issue in the processors performance evolution. Historically, the insertion of cache levels designed with SRAM (Static Random Access Memory) cells in the same processor technology node allowed to executed data and instructions access in a cycle of the clock, instead of the high time to access data from the hard drive memory. With the technology scaling, the area is no longer a relevant issue, allowing a large integration scale of cache levels inside the processors chip. However, power consumption rises as a high claim for many applications. Moreover, the aggressive scaling alongside the low supply voltages, large transistor density, and, high-frequency operation introduce new reliability issues, such as the high radiation effects sensitivity and multi-charge collection [1], [2].

The soft errors are the consequence of a transient pulse generated by the interaction of energetic particles near a sensitive region of a transistor when the collected charge (Q_{coll}) exceeds the critical charge (Q_{crit}). According to the energy of ionized particles hitting the silicon, the incident angle and the impact site, transient pulses can cause minor perturbations or even critical failures in the system behavior [3]. The main effects on memory elements are classified as Single Event Upsets (SEU) and characterized as a bit-flip on the memory element. Furthermore, the Static Noise Margin (SNM) is another measure to evaluate the stability of a memory cell, since it is the minimum noise voltage to flip the state of the cell.

The 6T cell is the most frequently used SRAM Cell on L1 cache design, and the traditional transistor arrangement is presented in Fig. 1(a). The 6T is composed of six transistors. The two most external to the cell are responsible for controlling of the access bitlines (BL and the complementary !BL) to internal nodes (Q and complementary QB). Its control is given through the signal sent by Wordline (WL). These transistors are of the NMOS type and are called M5-M6. The internal part of the cell has two transistors of the PMOS type, which has the function of raising the logical value of the cell, referred to M1-M2, and two other NMOS transistors by decreasing the logical signal, called M3-M4.

There are few hardened memory solutions in the literature, with particular reference to the CMOS DICE (Dual Interlocked Storage Cell) [4] [5], mainly because of the reduced increase in the area compared to traditional replication techniques as triple module redundancy (TMR). DICE circuit consists of two transistor groups whose layout on the crystal shape increases the cell stability against the impact of single particles, as shown in Fig. 1 (b). A fault on this cell does not take place if the particle only impacts the same group of transistors.

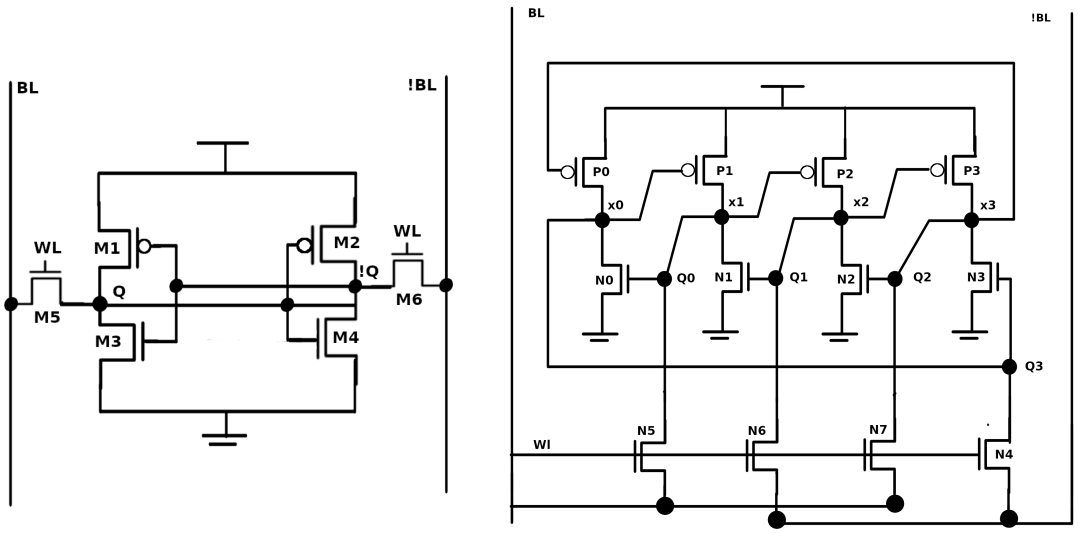
The DICE contains twelve transistors in which eight are used as inverter (P0-N0, P1-N1, P2-N2, P3-N3). Each inverter is connected with the next and previous inverter in the gate by the internal node X_i generating the robustness in the Hold. An example is the node X_0, if this node contains the logic value 1, DICE will open P1 and close N3, so the internals nodes X_1 and X_3 will receive the logical values 0 and 1 respectively. DICE circuit is a reference on reliability SRAM design. The two cells contain the Write and Pre-Charge circuits, found in the structure of SRAM architecture, and the 6T still has a Read Circuit. The auxiliary circuits descriptions are in Fig. 2.

This work presents the design of a DICE circuit on 7nm FinFET technology. The experiments show the impact on timing, power, static noise margin, and SEU robustness of this memory cell. The results are compared with the traditional 6T SRAM Cell to show the cost inserted in the design when radiation robustness is mandatory.

II. Methodology

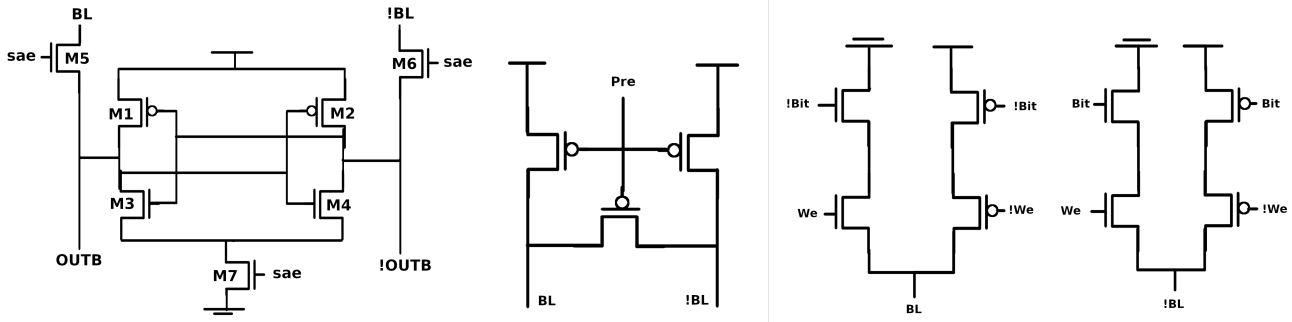
The design of the DICE circuit at electrical level adopts the ASAP 7nm FinFET Regular Threshold Voltage (RVT)model [6] operating between 0.7V and 0.4V. All devices are defined with one fin. To comparative and better understand the cell operation, this work analyses a 128 cells, with complementary circuits executing reading, writing, and hold operations. All evaluation was done through electrical simulations using Hspice Tool.

This work defines a sequence of operations, write0/read0/write1/read1 (w0/r0/w1/r1) to validate correct operation on the design. The waves for each simulation are found in Fig. 3. Initially, a write operation of the logical



(a) 6T SRAM Cell (b) Dice SRAM Cell

Fig. 1: 6T and DICE SRAM Cells



(a) 6T Read Circuit (b) Pre-Charge Circuit (c) Write Circuit

Fig. 2: Complementary circuits

value 0 is done, and, after a period of Hold, the value stored is read. Subsequently, the writing of the logical value 1 is performed. Again, after a period of hold, the value stored is read. The same sequence is employed to achieve reading and writing times, energy consumption, and, in the SEU simulation experiments.

Given an example of operation, the waves of DICE are segmented in two operations, which are writing and reading. The difference to write zero and one is described in the respective subsection, the same was done to read. Because of the differences in the structure present in 6T SRAM Cell, the value of bitlines to write are reversed compared with the DICE bitlines. Likewise, the reading varies in which bitline is taken to verify the stored value. To write zero, the signal wl must be one to access the DICE circuit. Afterward, the signals BL and $!BL$ needs to be one and zero, respectively, and to achieve these signals bit and we need to be one, the same case for the signal pre, that used to pre-charge the bitlines (BL,$!BL$) before the writing. The change to write one lies in the reverse values of the bitlines made by the signal bit, which must to be zero. Also, to perform the reading operation the wl must have one and both bitlines have to be one and the signal pre produce that and the fall voltage of BL or $!BL$ is required to determinate the stored value. To measure the Static Noise Margin, an independent voltage source, which is increased at a rate of 0.1%, is used to simulate a noise in a DC simulation. This source is connected to the target node and all the signals are defined to simulate the operation.

The Single Events are modeled as a transient current source [7]. All internal nodes of the SRAM cells are individually investigated to identify the sensible nodes considering negative charges (pulses in the format of 101) and positive charges (010 pulses). The cells are evaluated during the three operation states: hold, write and read. For read and hold operations, the experiments consider the cell holding values '0' and '1'. For the write operation, the experiments start with the cell holding the opposite value to be written in the cell. The evaluation of single events during the read and write operations shows that

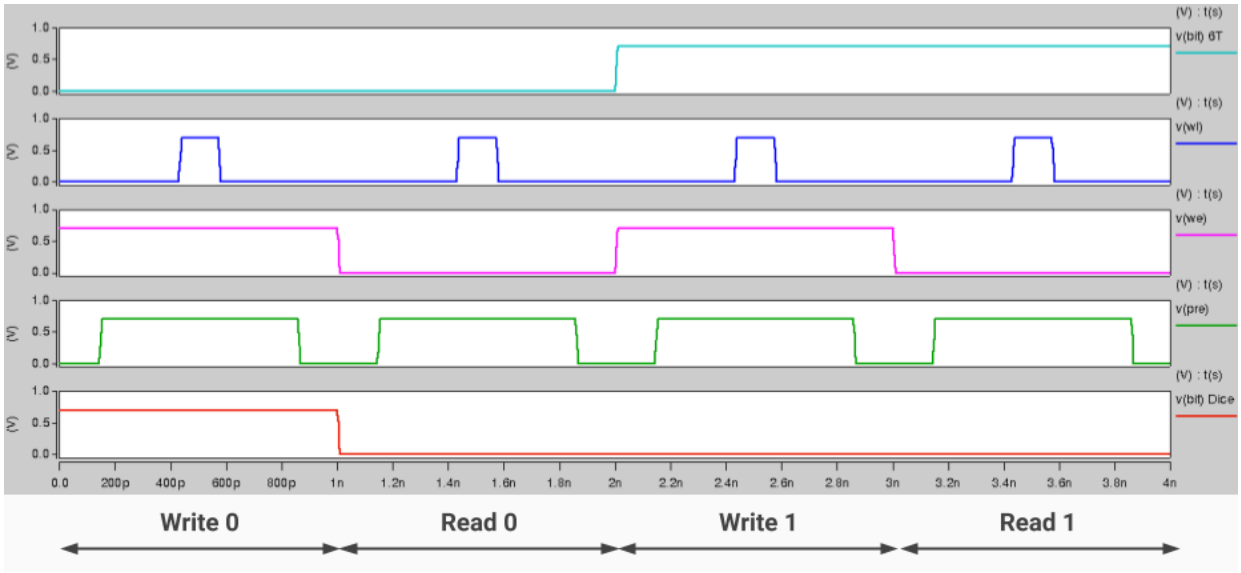


Fig. 3: Waves for SRAM validation comprising the write, read and hold operations.

there is a sensibility window where the faults can provoke a SEU in the cells, and that the LETth in this events may be significantly lower [8]. This work considers the Linear Energy Transfer (LET) threshold (LETth) to define the cell robustness. To obtain the LETth from the electrical simulations, it is necessary to get the current that causes a bit-flip in the cell and, calculate the Linear Energy Transfer (LET). The Table I shows the parameters used in this work to calculate the LET [9]. According to the energy spectrum of space particles, presented in Fig. 4, this work adopts as the limit of the tests the Solar Proton particles energy (up to 100 MeV/cm^2) [10].

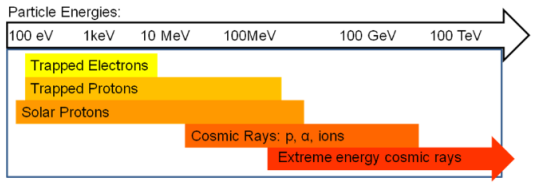


Fig. 4: Diagram of typical particle radiation spectra from the space environment [10]

TABLE I: Values of parameters to calculate the LET [9]

Parameter	Value
T_α	320ps
T_β	10ps
L	0.21nm

III. Results

The Table II presents the results for the nominal voltage. The 6T showed better timing and energy consumption, since its worst time was about 50% less than DICE and there was an 11% reduction in consumption. Regarding the noise margin, there was no significant difference, since the hold and read operations had a variation of less than 1% and only writing static noise margin had an improvement of 3% for DICE. Also, Read Static Noise Margin (RSNM) was the lowest for both cells in all simulations, in the case of DICE it is 54% worse on average. The great advantage in using DICE is in the robustness, given that only the reading was affected by the positive particles. However, all operations showed failures with the negative ones. Besides, the lowest LETth found was up to 85% higher than for 6T. The insertion of a failure in the reading operation had the worst result since it obtained a value 95% lower than the second least.

The Figure 5 reveals the results obtained and the trend lines for each operational voltage compared to the nominal one. Voltage scaling had a drastic impact on the results for both cells: positively reducing the energy consumption by 74%, but, negatively increasing the operating time, being 5.8 times the nominal voltage operation. The most significant influence of the voltage scaling was on writing timing, reaching 103.9 ps, 85% greater than the slowest reading time on the same voltage. About the noise margin, there was a decrease of at least 42% in the DICE when compared with the nominal value. Figure 6 shows the noise margins for each operation, given the voltage in absolute values.

Although DICE had worse results than the 6T in timing and energy consumption, it was superior in most robustness cases to SEU. On this, DICE maintained its robust behavior despite the reduction compared to the nominal operation. Since it is free of faults for positive particles in the hold and write operations, the reading operation remained the cells weak point and decreased by 58% about the reference. Figure 7 shows the strengths and weaknesses of DICE with the results obtained with the 6T operating at 0.7V, considering the worst-case scenario, with the smallest LET and margins and the worst times for each voltage.

TABLE II: Results at nominal voltage (0.7V)

Cell	Timing (ps)				Energy (fJ)	SNM (V)			LET threshold (MeV/cm^2)		
	Write 0	Read 0	Write 1	Read 1		Hold	Write	Read	Hold	Write	Read
6T	6.1363	8.9872	7.9678	8.988	20.8182	0.289	0.334	0.123	38.3	36.9	17.8
DICE	6.3008	17.753	8.1851	17.6555	23.396	0.290	0.344	0.123	611.0	92.3	32.8

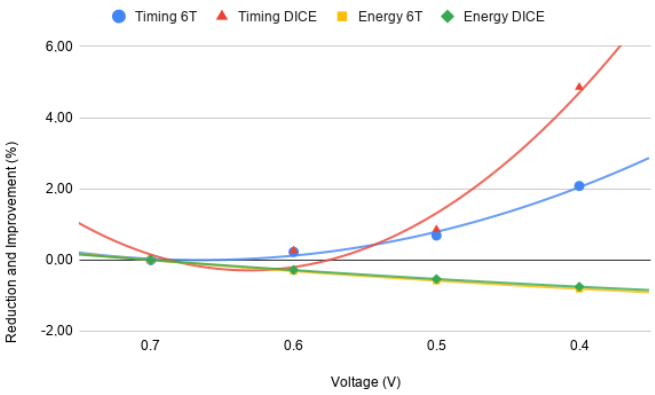


Fig. 5: Impact of voltage reduction on performance

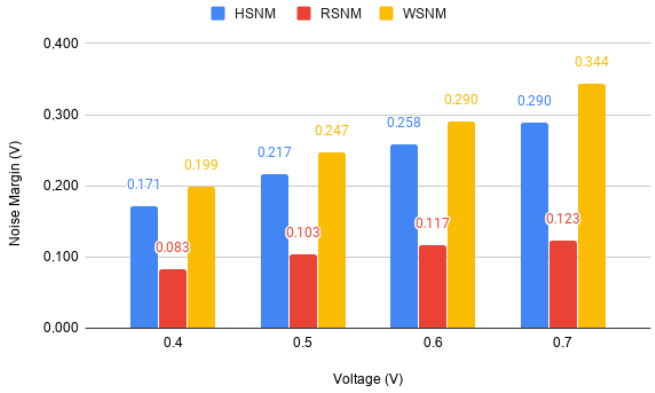


Fig. 6: DICE Noise Margins

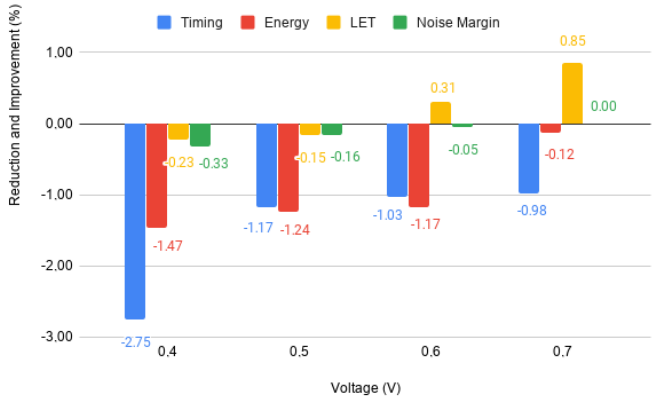


Fig. 7: Comparison between DICE and 6T

IV. Conclusion

This work provides an analysis of DICE operating at different voltages and the impacts of that. The operating times, energy consumption, LETth, and margins were evaluated. From the results obtained, the impact of a robust design and the reduction of tension on the characteristics of a memory cell, such as energy consumption and timing, are notable. On this, DICE presented worse results than the 6T in all cases, evidenced by Figure 5. However, by reducing the operating voltage of DICE to the maximum, the energy consumption had a value 74% lower than the nominal. Also, the cells robustness to positive particles remained despite the decrease, considering the hold, and write operations. Regarding noise margin, there was also a reduction in margins as the voltage is reduced, as can be seen in the Figure 6. In this way, DICE maintains its robust behavior despite the reduced voltage, having at most a reduction of 58% on the LETth and 33% on the RSNM compared with the nominal operation.

V. Acknowledgment

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